IN THE CLAIMS:

Claim 1. (**Currently Amended**) A method for prefetching a program stored in a memory, the method comprising the steps of:

reading the program from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the ~~branch~~ at least one instruction ~~or the call instruction~~ and including an address for ~~a branch destination~~ an instruction ~~or a call destination instruction~~;

detecting the pseudo instruction with a first unit;

reading the instruction from the memory in accordance with the address for the ~~branch destination~~ instruction ~~or the call destination instruction~~ with the first unit when the pseudo instruction is detected;

storing the instruction in a buffer; ~~and~~

executing the at least one instruction following the pseudo instruction without executing the pseudo instruction; and

executing the stored instruction with a second unit.

Claim 2. (**Previously Presented**) The method of claim 1, wherein the first unit includes a pseudo instruction detection unit connected in parallel with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit in parallel with the buffer.

Claim 3. (**Previously Presented**) The method of claim 1, wherein the buffer includes first and second buffers connected in parallel to the memory, and the method further comprising a step of storing the instruction read from the memory in the first buffer and storing the instruction included in the detected pseudo instruction in the second buffer.

Claim 4. (**Currently Amended**) The method of claim 3, further comprising the steps of:

identifying that the at least one instruction following the pseudo instruction has been transferred to the first buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction from the memory in accordance with the at least one instruction address with the first unit after the transfer of the at least one instruction to the first buffer has been identified.

Claim 5. (**Currently Amended**) The method of claim 4, further comprising the step of identifying that the corresponding instruction is stored in the second buffer in accordance with the ~~at least one instruction~~ address when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction is not stored in the second buffer.

Claim 6. (**Currently Amended**) The method of claim 1, further comprising the steps of:

identifying that the at least one instruction following the pseudo instruction has been transferred to the buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction and the data from the memory in accordance with ~~at least one instruction~~ the address with the first unit after the transfer of at least one instruction to the buffer has been identified.

Claim 7. (**Currently Amended**) The method of claim 6, further comprising the step of identifying that the corresponding instruction is stored in the buffer in accordance with the ~~at least one instruction~~ address with the first unit when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction is not stored in the buffer.

Claim 8. (**Currently Amended**) A microcontroller, comprising:

a buffer, connected to a memory, for storing a program read from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the ~~branch~~ at least one instruction ~~or the call instruction~~ and including an address for a ~~branch destination~~ an instruction ~~or a call destination instruction~~;

a first unit including,

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program read from the memory; and

an address control unit, connected to the memory and the pseudo instruction detection unit, for reading the instruction from the memory in accordance with the address for ~~a branch destination~~ the instruction ~~or a call destination instruction~~ when the pseudo instruction is detected and storing the instruction in the buffer; and

a second unit connected to the buffer, for executing the at least one instruction following the pseudo instruction without executing the pseudo instruction, wherein the second unit executes ~~executing~~ the instruction stored in the buffer.

Claim 9. (**Previously Presented**) The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel to the memory, wherein the first buffer stores the instruction read from the memory, and the second buffer stores the instruction included in the detected pseudo instruction.

Claim 10. (**Currently Amended**) The microcontroller of claim 9, wherein the address control unit identifies that the corresponding instruction is stored in the second buffer in accordance with the ~~at least one instruction~~ address when the pseudo instruction is detected and permits storage of the instruction in the second buffer when the corresponding instruction is not stored in the second buffer.

Claim 11. (**Previously Presented**) The microcontroller of claim 10, wherein the pseudo instruction detection unit is connected in parallel with the first buffer for the memory.

Claim 12. (**Currently Amended**) The microcontroller of claim 8, wherein the address control unit identifies that the corresponding instruction is stored in the buffer in accordance with the ~~at least one instruction~~ address when the pseudo instruction is detected and permits storage of the instruction in the buffer when the corresponding instruction is not stored in the buffer.

Claim 13. (**Previously Presented**) The microcontroller of claim 12, wherein the pseudo instruction detection unit is connected in parallel with the buffer for the memory.

Claim 14-24. (**Canceled**).

Claim 25. (**Previously Presented**) The method of claim 1, further comprising handling the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected.

Claim 26. (**Currently Amended**) The method of claim 1, further comprising the second unit ignoring an address for the pseudo instruction when receiving the address

for ~~a branch destination~~ the instruction ~~or a call destination instruction~~ to skip the pseudo instruction.

Claim 27. (**Cancelled**)

Claim 28. (**Previously Presented**) The microcontroller of claim 8, wherein the second unit handles the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected.

Claim 29. (**Currently Amended**) The microcontroller of claim 8, wherein the second unit ignores an address for the pseudo instruction when receiving the address for ~~a branch destination~~ the instruction ~~or a call destination instruction~~ to skip the pseudo instruction.

Claim 30. (**Currently Amended**) A method for prefetching a program stored in a memory, the method comprising the steps of:

reading the program from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the ~~branch~~ at least one instruction ~~or the call instruction~~ and including an address for ~~a branch destination~~ an instruction ~~or a call destination instruction~~;

detecting the pseudo instruction with a first unit;

prefetching the instruction in accordance with the ~~detection of the pseudo~~ instruction with the first unit when the pseudo instruction is detected; ~~and~~

handling the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected with a second unit; and

executing the at least one instruction following the pseudo instruction with the second unit without executing the pseudo instruction.

Claim 31. (**Currently Amended**) A method for prefetching a program stored in a memory, the method comprising the steps of:

reading the program from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the ~~branch~~ at least one instruction ~~or the call instruction~~ and including an address for ~~a branch destination~~ an instruction ~~or a call destination instruction~~;

detecting the pseudo instruction with a first unit when the pseudo instruction is detected;

prefetching the instruction in accordance with the detection of the pseudo instruction with the first unit; ~~and~~

when receiving the address for the ~~branch destination~~ instruction ~~or the call destination instruction~~ with a second unit, which is independent of the first unit, and skipping the pseudo instruction ~~and executing the prefetched instruction~~; and

executing the at least one instruction following the pseudo instruction without executing the pseudo instruction, and

executing the prefetched instruction.

Claim 32. (**Currently Amended**) An apparatus for prefetching a program stored in a memory, the apparatus comprising:

a first unit for reading the program from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the at least one instruction and including an address for ~~a branch destination~~ an instruction ~~or a call destination instruction~~, and wherein the first unit detects the pseudo instruction and prefetches the instruction when the pseudo instruction is detected; and

a second unit for executing a no-operation (NOP) operation in accordance with the detection of the pseudo instruction and executing the at least one instruction without executing the pseudo instruction.

Claim 33. (**Currently Amended**) An apparatus for prefetching a program stored in a memory, the apparatus comprising:

a first unit for reading the program from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the ~~branch~~ at least one instruction ~~or the call instruction~~ and including an address for ~~a branch destination~~ an

instruction ~~or a call destination instruction~~, and wherein the first unit detects the pseudo instruction and prefetches the instruction when the pseudo instruction is detected; and

a second unit for executing the prefetched instruction, wherein the second unit ignores an address for the pseudo instruction when receiving the address for the ~~branch destination~~ instruction ~~or the call destination instruction~~ to skip the pseudo instruction, and wherein the second unit executes the at least one instruction without executing the pseudo instruction.

Claim 34. (**Currently Amended**) An apparatus for prefetching a program stored in a memory, the apparatus comprising:

a first unit for reading the program from the memory, wherein the program includes a pseudo instruction and at least one ~~branch~~ instruction ~~or at least one call instruction~~, the pseudo instruction being arranged before the ~~branch~~ at least one instruction ~~or the call instruction~~ and including an address for ~~a branch destination~~ an instruction ~~or a call destination instruction~~, and wherein the first unit reads the instruction from the memory in accordance with the address for the ~~branch~~ instruction ~~or the call destination instruction~~ when the pseudo instruction is detected, wherein the first unit includes a buffer for storing the instruction; and

a second unit for executing the at least one instruction following the pseudo instruction without executing the pseudo instruction, wherein the second unit executes executing the stored instruction.

35. (**Currently Amended**) The method of claim 1, wherein the stored instruction is executed in a next cycle after the ~~branch~~ at least one instruction ~~or the call instruction~~ is executed.

36. (**Currently Amended**) A method for prefetching a program stored in a memory, the method comprising the steps of:

reading the program from the memory, wherein the program includes a pseudo instruction and at least one data calling instruction, the pseudo instruction being arranged before the data calling instruction and including an address for calling data;

detecting the pseudo instruction with a first unit;

reading the data from the memory in accordance with the address for the calling data with the first unit when the pseudo instruction is detected;

storing the data in a buffer; and

executing the data calling instruction with a second unit without executing the pseudo instruction.

37. (**New**) The method of claim 1, further comprising holding an address of at least one previous instruction when the pseudo instruction is detected.